	Application No.	Applicant(s)	m
	10/792,042	MAY ET AL.	
Notice of Allowability	Examiner	Art Unit	
	Vibol Tan	2819	
The MAILING DATE of this communication appear All claims being allowable, PROSECUTION ON THE MERITS IS (herewith (or previously mailed), a Notice of Allowance (PTOL-85) of NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGOT OF THE NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGOT OF THE NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGOT OF THE NOTICE O	OR REMAINS) CLOSED in this apport of the appropriate communication GHTS. This application is subject to	plication. If not included will be mailed in due co	l ourse. <b>THIS</b>
1. $\boxtimes$ This communication is responsive to <u>the phone interview or</u>	<u>12/20/2005</u> .		
2. The allowed claim(s) is/are <u>3-5,9-11,13-17,19 and 21-33</u> .			
3. ☐ Acknowledgment is made of a claim for foreign priority und a) ☐ All b) ☐ Some* c) ☐ None of the:			
1. Certified copies of the priority documents have			
2. Certified copies of the priority documents have	• • • • • • • • • • • • • • • • • • • •		
<ol><li>Copies of the certified copies of the priority doc</li></ol>	uments have been received in this i	national stage applicatio	n from the
International Bureau (PCT Rule 17.2(a)).			
* Certified copies not received:			
Applicant has THREE MONTHS FROM THE "MAILING DATE" of noted below. Failure to timely comply will result in ABANDONMETHIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		complying with the requi	irements
4. A SUBSTITUTE OATH OR DECLARATION must be submit INFORMAL PATENT APPLICATION (PTO-152) which gives			TICE OF
5. CORRECTED DRAWINGS ( as "replacement sheets") must	be submitted.		
(a) I including changes required by the Notice of Draftsperso	on's Patent Drawing Review (PTO-	948) attached	
1)  hereto or 2) to Paper No./Mail Date			
(b) ☐ including changes required by the attached Examiner's Paper No./Mail Date	Amendment / Comment or in the O	office action of	
Identifying indicia such as the application number (see 37 CFR 1.8 each sheet. Replacement sheet(s) should be labeled as such in the	84(c)) should be written on the drawir e header according to 37 CFR 1.121(c	igs in the front (not the bad).	ack) of
<ol> <li>DEPOSIT OF and/or INFORMATION about the depos attached Examiner's comment regarding REQUIREMENT F</li> </ol>			te the
Attachment(s)	5 Division of laterary D	ata at Asalisatian (DTO)	450)
1. Notice of References Cited (PTO-892)	5. Notice of Informal P	• •	152)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	<ol> <li>6. ☑ Interview Summary Paper No./Mail Dat</li> </ol>	(P10-413), e <b>12-20</b> -25	
<ol> <li>Information Disclosure Statements (PTO-1449 or PTO/SB/08 Paper No./Mail Date</li> </ol>			
Examiner's Comment Regarding Requirement for Deposit of Biological Material	8. 🛛 Examiner's Stateme	nt of Reasons for Allowa	ance
or biological material	9.  Other		
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Page 2

Application/Control Number: 10/792,042

Art Unit: 2819

## **EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with C. Bart Sullivan on 12/20/2005.

The application has been amended as follows:

Please cancel claim 6.

In claim 14, line 7, change "...the configuration memory or to the programmable input/output..." to "...the configuration memory <u>and</u> to the programmable input/output..."

In claim 15, line 7, change "...logic section or to the programmable input/output..." to "...logic section <u>and</u> to the programmable input/output..."

## Allowable Subject Matter

2. The following is an examiner's statement of reasons for allowance: in combination with other limitations of the claims, the cited prior arts fail to teach the active logic section comprises a gate array and an embedded logic device and the gate array and the embedded logic device have separate supply connections, as recited in amended claim 3; the cited prior arts also fail to teach each of the separate power supply connections for the active logic section, the configuration memory, and the programmable input/output section are selectable between at least two different voltage levels, as recited in amended claim 5; the embedded logic device is connected to a third

Art Unit: 2819

pair of the pins different from the first to receive power therefrom, as recited in amended claim 9; the cited prior arts also fail to teach the programmable input/output section is connected to a fourth pair of the pins different from the first and second to receive power therefrom, as recited in amended claim 11; the cited prior arts also fail to teach operating the device in a second mode of operation, in which power is supplied to the gate array of the active logic section and power is disconnected from the embedded logic device, as recited in amended claim 13; the cited prior arts also fail to teach the power supplied to the configuration memory and to the programmable input/output section comprises at least two selectable voltage levels, as recited in amended claim 14; the cited prior arts also fail to teach the power supplied to the active logic section or to the programmable input/output section comprises at least two selectable voltage levels, as recited in amended claim 15; and the cited prior arts also fail to teach a power control circuit configured to operate each of the selectable power supply connections to selectively supply different power supply voltages to the active logic circuit, the configuration memory, and the gate array in response to a predetermined mode of operation, as recited in claim 26.

3. Claims 3-5, 9-11, 13-17, 19 and 21-33 are now in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Application/Control Number: 10/792,042

Art Unit: 2819

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

> VIBOL TAN PRIMARY EXAMINER